REMARKS

Summary of Office Action

Claims 1-21 are pending in this application.

The specification has been objected to for various informalities.

Claims 8 and 12 have been objected to as being of improper dependent form. Claims 2 and 6 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

Claims 1-14 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Peng U.S. Patent No. 5,594,675 ("Peng"). Claim 15 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Washakowski et al. U.S. Patent Publication No. 2005/0238117 ("Washakowski"). Claims 16-21 have been rejected under 35 U.S.C. § 103(a) as being obvious from Washakowski in view of Peng.

Summary of Applicant's Reply

Applicant has amended the specification to correct various clerical errors and to update cross-references. No new matter has been added.

Applicant has amended claims 1, 2, 6, 8, 12 and 15, in order to more particularly define the claimed invention. No new matter has been added and the amendments are fully supported by the originally-filed specification.

Applicant respectfully traverses the Examiner's rejections.

The Specification

The Examiner objected to the title as allegedly not being descriptive.

Applicant has amended the title to recite: " DSP CIRCUITRY FOR SUPPORTING MULTI-CHANNEL APPLICATIONS BY SELECTIVELY SHIFTING DATA THROUGH REGISTERS." Applicant respectfully submits that the title, as amended, is descriptive and indicative of the claimed invention.

Reply to the Claim Objections

The Examiner objected to claims 8 and 12 as being of improper dependent form for failing to further limit the subject matter of the previous claims.

Applicant has amended claims 8 and 12 to place them in proper dependent forms. Applicant therefore respectfully requests that the objection to claims 8 and 12 be withdrawn.

Reply to the Section 112 Rejection

The Examiner rejected claims 2 and 6 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The Examiner stated that the use of "the same channel" is vague and unclear.

Applicant has amended claims 2 and 6 to more clearly define the claimed invention. Applicant therefore respectfully submits that claims 2 and 6 are no longer indefinite and requests that the rejection of these claims be withdrawn.

Reply to the Prior Art Rejection

Claims 1-14

The Examiner rejected claims 1-14 under 35 U.S.C. § 102(b) as being anticipated by Peng. Applicant respectfully traverses this rejection.

Applicant's invention, as defined by amended claim 1, is directed to DSP circuitry that independently processes a plurality of multi-channel data signals. The circuitry includes a plurality of columns of registers. Each column includes an input and a plurality of registers arranged in serial. The DSP circuitry includes interconnection circuitry that allows a value at the input of each column to be selectively routed to any register in the column.

Peng generally describes a digital FIR filter. FIG. 11 shows multiple selector circuits 735 each including a shift register 734-u for storing L tap coefficient values and a multiplexer 732-u connected to each shift register. The multiplexer can select either the tap coefficient value outputted from its own shift register or the value outputted from a previous selector circuit 735 via line 736. (Peng, FIG. 11, col. 17, lines 5-24.)

The Examiner alleges that Peng shows all the features of applicant's claim 1. Applicant respectfully disagrees.

Applicant respectfully submits that Peng does not show or suggest interconnection circuitry that allows a value at the input of each column to be selectively routed to any register in the column, as defined by claim 1. In the Peng device, each selector circuit includes only one multiplexer 732

for selecting, as input to the shift register, either the tap coefficient value outputted from its own shift register or the one outputted from a previous selector circuit. Nowhere does Peng show or suggest that multiplexer 732 can selectively route the input values, received from its own shift register or from another circuit, to any register 734 in the selector circuit. Thus, Peng does not show or suggest show all the features of applicant's claim 1.

Accordingly, applicant respectfully submits that independent claim 1 and claims 2-14 that depend, directly or indirectly therefrom, are allowable.

Claims 15-21

The Examiner rejected claim 15 under 35 U.S.C. § 102(b) as being anticipated by Washakowski. The Examiner rejected claims 16-21 under 35 U.S.C. § 103(a) as being obvious from Washakowski in view of Peng. Applicant respectfully traverses this rejection.

Applicant's invention, as defined by amended claim 15, is directed to DSP circuitry that supports multiple channels. The DSP circuitry includes tap delay line circuitry that includes registers for registering the data of each of the multiple channels such that the data of each channel is not mixed with the data of any other channel. The tap delay line circuitry includes an input and interconnection circuitry that allows a value received at the input to be selectively routed to any of said registers in said tap delay line circuitry.

Washakowski generally describes a baseband shaping device. The baseband shaping device includes a tapped delay

line 202I with a plurality of delay elements 203 coupled to an in-phase data bit stream. Each stage is coupled to a corresponding tap 205 of the delay line 202I. Eight individual registers 442Ia-g coupled in series represent the eight taps of the delay line in the filter. (Washakowski, FIGS. 2A and 4C; and page 2, paragraph 23 and page 4, paragraph 39.)

The Examiner alleges that Washakowski shows all the features of applicant's claim 15. Applicant respectfully disagrees.

Applicant respectfully submits that Washakowski does not show or suggest tap delay line circuitry that includes an input and interconnection circuitry that allows a value received at the input to be selectively routed to any of the registers in the tap delay line circuitry, as defined by claim 15. In the Washakowski device, the tap delay line circuitry includes registers coupled in series, where each register is only coupled to receive the value of its respective tap in the bit stream. Nowhere does Washakowski show or suggest interconnection circuitry that allows any of the registers to receive the value at the input of the tap delay line circuitry (i.e., the value at the first tap in the tap delay line circuitry). Thus, Washakowski does not show or suggest show all the features of applicant's claim 15.

Peng, cited as allegedly showing features of applicant's dependent claims, does not make up for the deficiencies in Washakowski relative to the rejection.

Accordingly, applicant respectfully submits that independent claim 15 and claims 16-21 that depend, directly or indirectly therefrom, are allowable.

Conclusion

The foregoing demonstrates that claims 1-21 are allowable. This application is therefore in condition for allowance. Reconsideration and prompt allowance are accordingly respectfully requested.

Respectfully submitted,

/Gall C. Gotfried/
Gall C. Gotfried
Registration No. 58,333
Agent for Applicant
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1211 Avenue of the Americas
New York, New York 10036-8704
Tel: (212) 596-9000